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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,707	01/24/2002	Teruhiko Kamigata	1614.1210	7916

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EXAMINER	
DONAGHUE, LARRY D	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,707	KAMIGATA ET AL.	
	Examiner	Art Unit	
	Larry D. Donaghue	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/27/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *ATTACHED*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-13 are presented for examination.

2. The drawings were received on 12/27/2005. These drawings are acceptable.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Slavenburg et al. (US 6,044,451) (here after Slavenburg).

Slavenburg anticipates a method for instruction processing executing (claim 1) on a computer, comprising: identifying a classification of a functional unit which can execute a basic instruction (Slavenburg, see column 1, lines 35 – 36, classification with issue slot for each of the functional units (Control, CONST, ALU, MUI, FPU and MEM) in the VLIW CPU); determining whether said basic instruction (Slavenburg – refers to basic instructions as "types of operations", as listed in parenthesis above) can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit (Slavenburg, column 4, lines 29 – 30, "Second issue slots all have some way of identifying which functional unit is to execute the operation) and said logical instruction slot (Slavenburg, teaches the validation and steps to ensure validation of the issue slot, see (Slavenburg, column 4, lines 29 – 30, "Second issue slots all have some way of identifying which functional unit is to execute the operation." Slavenburg refers to the instruction slot as an "issue slot". Note the mechanism Slavenburg implements to validate the contents of the issue slot is the imaginary slot Applicant calls the "logical instruction slot".) : and assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot (Slavenburg, column 6, lines 15 – 40, covers what the issue slot ultimately issues.

As to claim 2, Slavenburg taught the identifying is divided into identifying an instruction category of a basic instruction (Slavenburg, see column 1, lines 35 – 36, classification with issue slot for each of the functional units (Control, CONST, ALU, MUI, FPU and MEM) in the VLIW CPU), and identifying a classification of a functional unit which can execute said instruction category (Slavenburg, column 4, lines 29 – 30, "Second issue slots all have some way of identifying which functional unit is to execute the operation").

As to claim 3, Slavenburg taught prior to said assigning, checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots. assigning, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned (Slavenburg, column 4, lines 29 – 30, "Second issue slots all have some way of identifying which functional unit is to execute the operation) to other logical instruction slots (Slavenburg, see column 1, lines 35 – 36, classification with issue slot for each of the functional units (Control, CONST, ALU, MUI, FPU and MEM) in the VLIW CPU).

As to claim 4, Slavenburg taught prior to said assigning, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be

assigned (Slavenburg, column 4, lines 29 – 30, "Second issue slots all have some way of identifying which functional unit is to execute the operation)to other logical instruction slots (Slavenburg, see column 1, lines 35 – 36, classification with issue slot for each of the functional units (Control, CONST, ALU, MUI, FPU and MEM in the VLIW CPU as per the rejections prior above).

As to claim 5, Slavenburg taught said determining includes a step of identifying said logical instruction slot having a lowest numeral determined to be assignable. (Slavenburg, column 9, lines 9 – 11 – Interpretation – table look ups inherently begin with the lowest number index – Slavenburg uses table would locate the first available which in the reference would be the first (lowest address)).

As to claim 6, Slavenburg taught said assigning includes identifying said logical instruction slot having a lowest numeral determined to be assignable. (Slavenburg, column 9, lines 9 – 11 – Interpretation – table look ups inherently begin with the lowest number index – Slavenburg uses table would locate the first available which in the reference would be the first (lowest address)).

As to claim 7, Slavenburg taught said identifying, determining, checking and assigning are repeated for all instruction slots. (Slavenburg – in the rejection for claims 4 and 1 provides a method of identifying and determining, checking and assigning all instruction slots).

As to claim 8, Slavenburg taught said identifying, determining, checking and assigning are repeated for all instruction slots (Slavenburg – in the rejection for claims 4 and 1 provides a method of identifying and determining, checking and assigning all instruction slots).

Claims 9-12 fail to teach or define above or beyond claims 1-8 and are rejected for the reasons set forth above.

5. Claim 13 is rejected under 35 U.S.C. 102(a) as being anticipated by Miyake et al. (EP 1,089,168).

Miyake et al. taught arranging, via computer, variable-length instructions to be executed in an order in a logical instruction slot; and verifying an arrangement of the variable-length instructions (para. 67-69, figure 9).

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rozas	6,738,893
Faraboschi et al.	5,930,508

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Larry D. Donaghue whose telephone number is 571-272-3962. The examiner can normally be reached on M-F 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).